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DyCaPPON: Dynamic circuit and packet passive optical network

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ABSTRACT

Dynamic circuits are well suited for applications that require predictable service with a constant bit rate for a prescribed period of time, such as cloud computing and e-science applications. Past research on upstream transmission in passive optical networks (PONs) has mainly considered packet-switched traffic and has focused on optimizing packet-level performance metrics, such as reducing mean delay. This study proposes and evaluates a dynamic circuit and packet PON (DyCaPPON) that provides dynamic circuits along with packet-switched service. DyCaPPON provides (i) flexible packet-switched service through dynamic bandwidth allocation in periodic polling cycles, and (ii) consistent circuit service by allocating each active circuit a fixed-duration upstream transmission window during each fixed-duration polling cycle. We analyze circuit-level performance metrics, including the blocking probability of dynamic circuit requests in DyCaPPON through a stochastic knapsack-based analysis. Through this analysis we also determine the bandwidth occupied by admitted circuits. The remaining bandwidth is available for packet traffic and we conduct an approximate analysis of the resulting mean delay of packet traffic. Through extensive numerical evaluations and verifying simulations we demonstrate the circuit blocking and packet delay trade-offs in DyCaPPON.

1. Introduction

Optical networks have traditionally employed three main switching paradigms, namely circuit switching, burst switching, and packet switching, which have extensively studied respective benefits and limitations [1–4]. In order to achieve the predictable network service of circuit switching while enjoying some of the flexibilities of burst and packet switching, *dynamic circuit switching* has been introduced [5]. Dynamic circuit switching can be traced back to research toward differentiated levels of blocking rates of calls [6]. Today, a plethora of network applications ranging from the migration of data and computing work loads to cloud storage and computing [7] as well as high-bit rate e-science applications, e.g., for remote scientific collaborations, to big data applications of governments, private organizations, and households are well supported by dynamic circuit switching [5]. Both commercial and research/education network providers have recently started to offer optical dynamic circuit switching services [8,9].

While dynamic circuit switching has received growing research attention in core and metro networks [9–17],

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mechanisms for supporting dynamic circuit switching in passive optical networks (PONs), which are a promising technology for network access [18–22], are largely an open research area. As reviewed in Section 2, PON research on the upstream transmission direction from the distributed Optical Network Units (ONUs) to the central Optical Line Terminal (OLT) has mainly focused on mechanisms supporting packet-switched transport [23–25]. While some of these packet-switched transport mechanisms support quality of service akin to circuits through service differentiation mechanisms, to the best of our knowledge there has been no prior study of circuit-level performance in PONs, e.g., the blocking probability of circuit requests for a given circuit request rate and a circuit holding time.

In this paper, we present the first circuit-level performance study of a PON with polling-based medium access control. We make three main original contributions towards the concept of efficiently supporting both *Dy*namic *C*ircuit *a*nd *P*acket traffic in the upstream direction on a *PON*, which we refer to as *DyCaPPON*:

- We propose a novel DyCaPPON polling cycle structure that exploits the dynamic circuit transmissions to mask the round-trip propagation delay for dynamic bandwidth allocation to packet traffic.
- We develop a stochastic knapsack-based model of DyCaPPON to evaluate the circuit-level performance, including the blocking probabilities for different classes of circuit requests.
- We analyze the bandwidth sharing between circuit and packet traffic in DyCaPPON and evaluate packet-level performance, such as mean packet delay, as a function of the circuit traffic.

This article is organized as follows. We first review related work in Section 2. In Section 3, we describe the considered access network structure and define both the circuit and packet traffic models as well as the corresponding circuit- and packet-level performance metrics. In Section 4, we introduce the DyCaPPON polling cycle structure and outline the steps for admission control of dynamic circuit requests and dynamic bandwidth allocation to packet traffic. In Section 5, we analyze the performance metrics relating to the dynamic circuit traffic, namely the blocking probabilities for the different circuit classes. We also analyze the bandwidth portion of a cycle consumed by active circuits, which in turn determines the bandwidth portion available for packet traffic, and analyze the resulting mean delay for packet traffic. In Section 6, we validate numerical results from our analysis with simulations and present illustrative circuit- and packet-level performance results for DyCaPPON. We summarize our conclusions in Section 7 and outline future research directions towards the DyCaPPON concept.

2. Related work

The existing research on upstream transmission in passive optical access networks has mainly focused on packet traffic and related packet-level performance metrics. A number of studies have primarily focused on differentiating the packet-level QoS for different classes of packet traffic, e.g., [26–34]. In contrast to these studies, we consider only best effort service for the packet traffic in this article. In future work, mechanisms for differentiation of packet-level QoS could be integrated into the packet partition (see Section 4) of the DyCaPPON polling cycle.

The needs of applications for transmission with predictable quality of service have led to various enhancements of packet-switched transport for providing quality of service (QoS). A few studies, e.g., [35–40], have specifically focused on providing deterministic QoS, i.e., absolute guarantees for packet-level performance metrics, such as packet delay or jitter. Several studies have had a focus on the efficient integration of deterministic QoS mechanisms with one or several lower-priority packet traffic classes in polling-based PONs, e.g., [41–47]. The resulting packet scheduling problems have received particular attention [48–50]. Generally, these prior studies have found that fixed-duration polling cycles are well suited for supporting consistent QoS service. Similar to prior studies, we employ fixed-duration polling cycles in DyCaPPON, specifically on a PON with a single-wavelength upstream channel.

The prior studies commonly considered traffic flows characterized through leaky-bucket parameters that bound the long-term average bit rate as well as the size of sudden traffic bursts. Most of these studies include admission control, i.e., admit a new traffic flow only when the packet-level performance guarantees can still be met with the new traffic flow added to the existing flows. However, the circuit-level performance, i.e., the probability of blocking (i.e., denial of admission) of a new request has not been considered. In contrast, the circuits in DyCaPPON provide absolute QoS to constant bit rate traffic flows without bursts and we analyze the probability of new traffic flows (circuits) being admitted or blocked. This flow (circuit) level performance is important for network dimensioning and providing QoS at the level of traffic flows.

For completeness, we briefly note that a PON architecture that can provide circuits to ONUs through orthogonal frequency division multiplexing techniques on the physical layer has been proposed in [51]. Our study, in contrast, focuses on efficient medium access control techniques for supporting circuit traffic. A QoS approach based on burst switching in a PON has been proposed in [52]. To the best of our knowledge, circuit level performance in PONs has so far only been examined in [53] for the specific context of optical code division multiplexing [54].

We also note for completeness that large file transmissions in optical networks have been examined in [55], where scheduling of large data file transfers on the optical grid network is studied, in [56], where parallel transfer over multiple network paths is examined, and in [57], where files are transmitted in a burst mode, i.e., sequentially.

Sharing of a general time-division multiplexing (TDM) link by circuit and packet traffic has been analyzed in several studies, e.g. [58–62]. These queueing theoretic analyses typically employed detailed Markov models and become computationally quite demanding for high-speed links. Also, these complex existing models considered a given node with local control of all link transmissions. In contrast, we develop a simple performance model for

the distributed transmissions of the ONUs that are coordinated through polling-based medium access control in DyCaPPON. Our DyCaPPON model is accurate for the circuits and approximate for the packet service. More specifically, we model the dynamics of the circuit traffic, which is given priority over packet traffic up to an aggregate circuit bandwidth of C_c in DyCaPPON, with accurate stochastic knapsack modeling techniques in Section 5.1. In Section 5.2, we present an approximate delay model for the packet traffic, which can consume the bandwidth left unused by circuit traffic in DyCaPPON.

3. System model

3.1. Network structure

We consider a PON with J ONUs attached to the OLT with a single downstream wavelength channel and a single upstream wavelength channel [25,63]. We denote C for the transmission bit rate (bandwidth) of a channel (bits/s). We denote τ (s) for the one-way propagation delay between the OLT and the equidistant ONUs. We denote Γ (s) for the fixed duration of a polling cycle. The model notations are summarized in Table 1.

3.2. Traffic models

For circuit traffic, we consider K classes of circuits with bandwidths $\mathbf{b}=(b_1,\ b_2,\ldots,b_K)$. We denote λ_c (requests/s) for the aggregate Poisson process arrival rate of circuit requests. A given circuit request is for a circuit of class k, $k=1,2,\ldots,K$, with probability p_k. We denote the mean circuit bit rate of the offered circuit traffic by $\overline{b}=\sum_{k=1}^{K}p_k b_k$. We model the circuit holding time (duration) as an exponential random variable with mean $1/\mu$. We denote the resulting offered circuit traffic intensity (load) by $\chi:=\lambda_c\overline{b}/(\mu C)$.

For packet traffic, we denote $\overline{P}$ and σ_p^2 for the mean and the variance of the packet size (in bit), respectively. We denote λ_p for the aggregate Poisson process arrival rate (packets/s) of packet traffic across the J ONUs and denote $\pi:=\overline{P}\lambda_p/C$ for the packet traffic intensity (load).

Throughout, we define the packet sizes and circuit bit rates to include the per-packet overheads, such as the preamble for Ethernet frames and the interpacket gap, as well as the packet overheads when packetizing circuit traffic for transmission.

Table 1
Main model notations.

Network architecture	
C	Transmission rate [bit/s] of upstream channel
C_c	Transmission rate limit for circuit service, $C_c \le C$
J	Number of ONUs
τ	One-way propagation delay [s]
Traffic model	
$\mathbf{b}=(b_1,\ldots,b_K)$	Bit rates [bit/s] for circuit classes $k=1,2,\ldots,K$
λ_c	Aggregate circuit requests arrival rate [circuits/s]
p_k	Prob. that a request is for circuit type k
$\overline{b}=\sum_{k=1}^{K}p_k b_k$	Mean circuit bit rate [bit/s] of offered circuit traffic
$1/\mu$	Mean circuit holding time [s/circuit]
$\chi=\frac{\lambda_c\overline{b}}{\mu C}$	Offered circuit traffic intensity (load)
$\overline{P}$, σ_p^2	Mean [bit] and variance of packet size
$\pi=\frac{\lambda_p\overline{P}}{C}$	Packet traffic intensity (load); λ_p is agg. packet generation rate [packets/s] at all J ONUs
Polling protocol	
Γ	Total cycle duration [s], constant
Ξ	Cycle duration (rand. var.) occupied by circuit traffic
ω	Mean per-cycle overhead time [s] for upstream transmissions (report transm. times, guard times)
Stochastic knapsack model for circuits	
$\mathbf{n}=(n_1,\ldots,n_K)$	State vector of numbers of circuits of class k
$\beta=\mathbf{n}\cdot\mathbf{b}$	Aggregate bandwidth of active circuits
$q(\beta)$	Equilibrium probability for active circuits having aggregate bandwidth β
Performance metrics	
B_k	Blocking probability for circuit class k
D	Mean packet delay [s]

3.3. Performance metrics

For circuit traffic, we consider the blocking probability B_k, $k=1,2,\ldots,K$, i.e., the probability that a request for a class k circuit is blocked, i.e., cannot be accommodated within the transmission rate limit for circuit service C_c. We define the average circuit blocking probability as $\overline{B}=\sum_{k=1}^{K}p_k B_k$. For packet traffic, we consider the mean packet delay D defined as the time period from the instant of packet arrival at the ONU to the instant of complete delivery of the packet to the OLT.

4. DyCaPPON upstream bandwidth management

4.1. Overview of cycle and polling structure

In order to provide circuit traffic with consistent upstream transmission service with a fixed circuit bandwidth, DyCaPPON employs a polling cycle with a fixed duration Γ (s). An active circuit with bandwidth b is allocated an upstream transmission window of duration $b\Gamma/C$ in every cycle. Thus, by transmitting at the full upstream channel bit rate C for duration $b\Gamma/C$ once per cycle of duration Γ, the circuit experiences a transmission bit rate (averaged over the cycle duration) of b. We let $\Xi(n)$ denote the aggregate of the upstream transmission windows of all active circuits in the PON in cycle n, and refer to $\Xi(n)$ as the circuit partition duration. We refer to the remaining duration $\Gamma-\Xi(n)$ as the packet partition of cycle n.

As illustrated in Fig. 1, a given cycle n consists of the circuit partition followed by the packet partition. During the packet partition of each cycle, each ONU sends a report message to the OLT. The report message signals new circuit requests as well as the occupancy level (queue depth) of the packet service queue in the ONU to the OLT. The signaling information for the circuit requests, i.e., requested circuit bandwidth and duration, can be carried in the Report message of the MPCP protocol in EPONs with similar modifications as used for signaling information for operation on multiple wavelength channels [64].

Specifically, for signaling dynamic circuit requests, an ONU report in the packet partition of cycle $n-1$ carries circuit requests generated since the ONU's preceding report

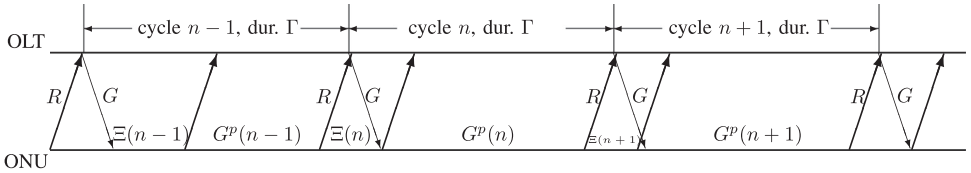

Fig. 1. An upstream cycle n has fixed duration Γ and has a circuit partition of duration $\Xi(n)$ (that depends on the bandwidth demands of the accepted circuits) while a packet partition occupies the remaining cycle duration $\Gamma-\Xi(n)$. The exact duration $G_p(n)$ of the packet partition in cycle n is evaluated in Eq. (2). Each ONU sends a report during each packet partition. Packet traffic reported in cycle $n-1$ is served in the packet partition of cycle n (if there is no backlog). A circuit requested in cycle $n-1$ starts in the circuit partition of cycle $n+1$. The 2τ round-trip propagation delay between the last ONU report (R) of a cycle $n-1$ and the first packet transmission following the grant (G) of the next cycle n is masked by the circuit partition, provided $\Xi(n)>2\tau$.

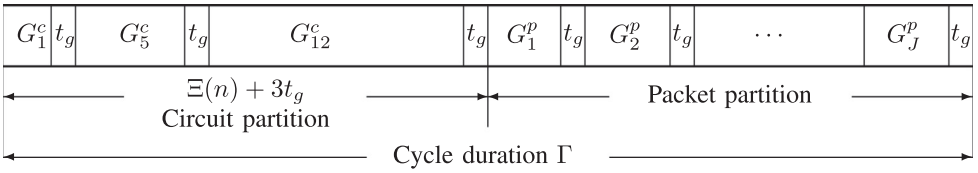

Fig. 2. Detailed example illustration of an upstream transmission cycle n: ONUs 1, 5, and 12 have active circuits with bandwidths resulting in circuit grant durations G_1^c, G_5^c, and G_{12}^c. Each of the J ONUs is allocated a packet grant of duration G_j^p according to the dynamic packet bandwidth allocation based on the reported packet traffic; the packet grant accommodates at least the ONU report (even if there is no payload packet traffic).

in cycle $n-2$. The report reaches the OLT by the end of cycle $n-1$ and the OLT executes circuit admission control as described in Section 4.2. The ONU is informed about the outcome of the admission control (circuit is admitted or blocked) in the gate message that is transmitted on the downstream wavelength channel at the beginning of cycle n. In the DyCaPPON design, the gate message propagates downstream while the upstream circuit transmissions of cycle n are propagating upstream. Thus, if the circuit was admitted, the ONU commences the circuit transmission with the circuit partition of cycle $n+1$.

For signaling packet traffic, the ONU report in the packet partition of cycle $n-1$ carries the current queue depth as of the report generation instant. Based on this queue depth, the OLT determines the effective bandwidth request and bandwidth allocation as described in Section 4.3. The gate message transmitted downstream at the beginning of cycle n informs the ONU about its upstream transmission window in the packet partition of cycle n.

As illustrated in Fig. 1, in the DyCaPPON design, the circuit partition is positioned at the beginning of the cycle, in an effort to mitigate the idle time between the end of the packet transmissions in the preceding cycle and the beginning of the packet transmissions of the current cycle. In particular, when the last packet transmission of cycle $n-1$ arrives at the OLT at the end of cycle $n-1$, the first packet transmission of cycle n can arrive at the OLT at the very earliest one roundtrip propagation delay (plus typically negligible processing time and gate transmission time) after the beginning of cycle n. If the circuit partition duration $\Xi(n)$ is longer than the roundtrip propagation delay 2τ, then idle time between packet partitions is avoided. On the other hand, if $\Xi(n)<2\tau$, then there an idle channel period of duration $2\tau-\Xi(n)$ between the end of the circuit partition and the beginning of the packet partition in cycle n.

Note that this DyCaPPON design trades off lower responsiveness to circuit requests for the masking of the roundtrip propagation delay. Specifically, when an ONU signals a dynamic circuit request in the report message in cycle $n-1$, it can at the earliest transmit circuit traffic in cycle $n+1$. On the other hand, packet traffic signaled in the report message in cycle $n-1$ can be transmitted in the next cycle, i.e., cycle n.

Fig. 2 illustrates the structure of a given cycle in more detail, including the overheads for the upstream transmissions. Each ONU that has an active circuit in the cycle requires one guard time of duration t_g in the circuit partition. Thus, with η denoting the number of ONUs with active circuits in the cycle, the duration of the circuit partition is $\Xi(n)+\eta t_g$. In the packet partition, each of the J ONUs transmits at least a report message plus possibly some data upstream, resulting in an overhead of $J(t_R+t_g)$. Thus, the overhead per cycle is

$$\omega_o=\eta t_g+J(t_R+t_g). \tag{1}$$

The resulting aggregate limit of the transmission windows for packets in cycle n is

$$G^p(n)=\Gamma-\max\{2\tau,\ \Xi(n)\}-\omega_o. \tag{2}$$

4.1.1. Low-packet-traffic mode polling

If there is little packet traffic, the circuit partition $\Xi(n)$ and the immediately following packet transmission phase denoted P1 in Fig. 3 may leave significant portions of the fixed-duration cycle idle. In such low-packet-traffic cycles, the OLT can launch additional polling rounds denoted P2, P3, and P4 in Fig. 3 to serve newly arrived packets with low delay. Specifically, if all granted packet upstream transmissions have arrived at the OLT and there is more than $J(t_R+t_g)+2\tau$ time remaining until the end of the cycle (i.e., the beginning of the arrival of the next circuit partition Ξ_{n+1}) at the OLT, then the OLT can launch another polling round.

4.2. Dynamic circuit admission control

For each circuit class k, $k=1,2,\ldots,K$, the OLT tracks the number n_k of currently active circuits, i.e., the OLT tracks

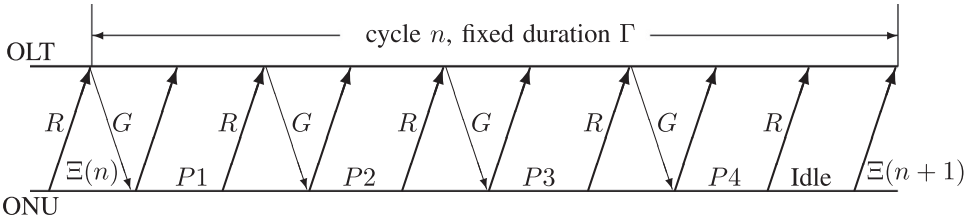

Fig. 3. Illustration of low-packet-traffic mode polling: if transmissions from all ONUs in the packet phase P1 following the circuit partition $\Xi(n)$ reach the OLT more than 2τ before the end of the cycle, the OLT can launch additional packet polling rounds P2, P3, and P4 to serve newly arrived packet traffic before the next circuit partition $\Xi(n+1)$.

the state vector $\mathbf{n}:=(n_1,\ldots,n_k)$ representing the numbers of active circuits. Taking the inner product of $\mathbf{n}$ with the vector $\mathbf{b}:=(b_1,\ldots,b_k)$ representing the bit rates of the circuit classes gives the currently required aggregate circuit bandwidth

$$\beta=\mathbf{b}\cdot\mathbf{n}=\sum_{k=1}^{K}b_k n_k, \tag{3}$$

which corresponds to the circuit partition duration

$$\Xi(n)=\frac{\beta\Gamma}{C}. \tag{4}$$

For a given limit C_c, $C_c\le C$, of bandwidth available for circuit service, we let $\mathcal{S}$ denote the state space of the stochastic knapsack model [65] of the dynamic circuits, i.e.,

$$\mathcal{S}:=\{\mathbf{n}\in I^K:\mathbf{b}\cdot\mathbf{n}\le C_c\}, \tag{5}$$

where I is the set of non-negative integers.

For an incoming ONU request for a circuit of class k, we let $\mathcal{S}_k$ denote the subset of the state space $\mathcal{S}$ that can accommodate the circuit request, i.e., has at least spare bandwidth b_k before reaching the circuit bandwidth limit C_c. Formally,

$$\mathcal{S}_k:=\{\mathbf{n}\in\mathcal{S}:\mathbf{b}\cdot\mathbf{n}\le C_c-b_k\}. \tag{6}$$

Thus, if presently $\mathbf{n}\in\mathcal{S}_k$, then the new class k circuit can be admitted; otherwise, the class k circuit request must be rejected (blocked).

4.3. Packet traffic dynamic bandwidth allocation

With the offline scheduling approach [25] of DyCaP-PON, the reported packet queue occupancy corresponds to the duration of the upstream packet transmission windows $R_j, j=1,2,\ldots,J$, requested by ONU j. Based on these requests, and the available aggregate packet upstream transmission window G^p (2), the OLT allocates upstream packet transmission windows with durations G_j^p, $j=1,2,\ldots,J$, to the individual ONUs.

The problem of fairly allocating bandwidth so as to enforce a maximum cycle duration has been extensively studied for the Limited grant sizing approach [27,66], which we adapt as follows. We set the packet grant limit for cycle n to

$$G_{\max}(n)=\frac{G^p(n)}{J}. \tag{7}$$

If an ONU requests less than the maximum packet grant duration $G_{\max}(n)$, it is granted its full request and the excess bandwidth (i.e., difference between $G_{\max}(n)$ and allocated grant) is collected by an excess bandwidth distribution mechanism. If an ONU requests a grant duration longer than $G_{\max}(n)$, the OLT allocates this maximum grant duration, plus a portion of the excess bandwidth according to the equitable distribution approach with a controlled excess allocation bound [66,67].

With the Limited grant sizing approach, there is commonly an unused slot remainder of the grant allocation to ONUs [68–70] due to the next queued packet not fitting into the remaining granted transmission window. We model this unused slot remainder by half of the average packet size $\overline{P}$ for each of the J ONUs. Thus, the total mean unused transmission window duration in a given cycle is

$$\omega_u=\frac{J\overline{P}}{2C}. \tag{8}$$

5. Performance analysis

5.1. Circuit traffic

5.1.1. Request blocking

In this section, we employ techniques from the analysis of stochastic knapsacks [65] to evaluate the blocking probabilities B_k of the circuit class. We also evaluate the mean duration of the circuit partition Ξ, which governs the mean available packet partition duration G^p, which in turn is a key parameter for the evaluation of the mean packet delay in Section 5.2.2.

The stochastic knapsack model [65] is a generalization of the well-known Erlang loss system model to circuits with heterogeneous bandwidths. In brief, in the stochastic knapsack model, objects of different classes (sizes) arrive to a knapsack of fixed capacity (size) according to a stochastic arrival process. If a newly arriving object fits into the currently vacant knapsack space, it is admitted to the knapsack and remains in the knapsack for some random holding time. After the expiration of the holding time, the object leaves the knapsack and frees up the knapsack space that it occupied. If the size of a newly arriving object exceeds the currently vacant knapsack space, the object is blocked from entering the knapsack, and is considered dropped (lost).

We model the prescribed limit C_c on the bandwidth available for circuit service as the knapsack capacity. The requests for circuits of bandwidth b_k, $k=1,2,\ldots,K$, arriving according to a Poisson process with rate $p_k\lambda_c$ are modeled as the objects seeking entry into the knapsack. An admitted circuit of class k occupies the bandwidth

(knapsack space) b_k for an exponentially distributed holding time with mean $1/\mu$.

We denote $\mathcal{S}(\beta)$ for the set of states $\mathbf{n}$ that occupy an aggregate bandwidth β, $0 \le \beta \le C_c$, i.e.,

$$\mathcal{S}(\beta) := \{\mathbf{n} \in \mathcal{S} : \mathbf{b} \cdot \mathbf{n} = \beta\}. \tag{9}$$

Let $q(\beta)$ denote the equilibrium probability of the currently active circuits occupying an aggregate bandwidth of β. Through the recursive Kaufman–Roberts algorithm [65, p. 23], which is given in the Appendix, the equilibrium probabilities $q(\beta)$ can be computed with a time complexity of $O(C_c K)$ and a memory complexity of $O(C_c + K)$.

The blocking probability B_k, $k = 1, 2, \ldots, K$ is obtained by summing the equilibrium probabilities $q(\beta)$ of the sets of states that have less than b_k available circuit bandwidth, i.e.,

$$B_k = \sum_{\beta = C_c - b_k + 1}^{C_c} q(\beta). \tag{10}$$

We define the average circuit blocking probability

$$\overline{B} = \sum_{k=1}^{K} p_k B_k. \tag{11}$$

5.1.2. Aggregate circuit bandwidth

The performance evaluation for packet delay in Section 5.2 requires taking expectations over the distribution $q(\beta)$ of the aggregate bandwidth β occupied by circuits. In preparation for these packet evaluations, we define $\mathbb{E}_\beta[f(\beta)]$ to denote the expectation of a function f of the random variable β over the distribution $q(\beta)$, i.e., we define

$$\mathbb{E}_\beta[f(\beta)] = \sum_{\beta=0}^{C_c} f(\beta) q(\beta). \tag{12}$$

With this definition, the mean aggregate bandwidth of the active circuits is obtained as

$$\overline{\beta} = \mathbb{E}_\beta[\beta] = \sum_{\beta=0}^{C_c} \beta q(\beta). \tag{13}$$

Note that by taking the expectation of (4), the corresponding mean duration of the circuit partition is $\overline{\Xi} = \mathbb{E}_\beta[\beta\Gamma/C] = \overline{\beta}\Gamma/C$.

5.1.3. Delay and delay variation

In this section we analyze the delay and delay variations experienced by circuit traffic as it traverses a DyCaPPON network from ONU to OLT. Initially we ignore delay variations, i.e., we consider that a given circuit with bit rate b has a fixed position for the transmission of its $b\Gamma$ bits in each cycle. Three delay components arise: the "accumulation/dispersal" delay of Γ for the $b\Gamma$ bits of circuit traffic that are transmitted per cycle. Note that the first bit arriving to form a "chunk" of $b\Gamma$ bits experiences the delay Γ at the ONU, waiting for subsequent bits to "fill up (accumulate)" the chunk. The last bit of a chunk experiences essentially no delay at the ONU, but has to wait for a duration of Γ at the OLT to "send out (disperse)" the chunk at the circuit bit rate b. The other delay components are the transmission delay of $b\Gamma/C$ and the propagation delay τ. Thus, the total delay is

$$\Gamma\left(1 + \frac{b}{C}\right) + \tau. \tag{14}$$

Circuit traffic does not experience delay variations (jitter) in DyCaPPON as long as the positions (in time) of the circuit transmissions in the cycle are held fixed. When an ongoing circuit is closing down or a new circuit is established, it may become necessary to rearrange the transmission positions of the circuits in the cycle in order to keep all circuit transmissions within the circuit partition at the beginning of the cycle and avoid idle times during the circuit partition. Adaptations of packing algorithms [71] could be employed to minimize the shifts in transmission positions. Note that for a given circuit service limit C_c, the worst-case delay variation for a given circuit with rate b is less than $\Gamma(C_c - b)/C$ as the circuit could at the most shift from the beginning to the end of the circuit partition of maximum duration $\Gamma C_c/C$.

5.2. Packet traffic

5.2.1. Stability limit

Inserting the circuit partition duration Ξ from (4) into the expression for the aggregate limit G^p on the transmission window for packets in a cycle from (2) and taking the expectation $\mathbb{E}_\beta[\cdot]$ with respect to the distribution of the aggregate circuit bandwidth β, we obtain

$$\overline{G^p} = \Gamma - \mathbb{E}_\beta\left[\max\left\{2\tau, \frac{\beta\Gamma}{C}\right\}\right] - \omega_o. \tag{15}$$

Considering the unused slot remainder ω_u (8), the mean portion of a cycle available for upstream packet traffic transmissions is limited to

$$\pi_{\max} = 1 - E_\beta\left[\max\left\{\frac{2\tau}{\Gamma}, \frac{\beta}{C}\right\}\right] - \frac{\omega_o + \omega_u}{\Gamma}. \tag{16}$$

That is, the packet traffic intensity π must be less than $\pi_{\max}$ for stability of the packet service, i.e., for finite packet delays.

5.2.2. Mean delay

In this section, we present for stable packet service an approximate analysis of the mean delay D of packets transmitted during the packet partition. In DyCaPPON, packets are transmitted on the bandwidth that is presently not occupied by admitted circuits. Thus, fluctuations in the aggregate occupied circuit bandwidth β affect the packet delays. If the circuit bandwidth β is presently high, packets experience longer delays than for presently low circuit bandwidth β. The aggregated occupied circuit bandwidth β fluctuates as circuits are newly admitted and occupy bandwidth and as existing circuits reach the end of their holding time and release their occupied bandwidth. The time scale of these fluctuations of β increases as the average circuit holding time $1/\mu$ increases, i.e., as the circuit departure rate μ decreases (and correspondingly, the circuit request arrival rate λ decreases for a given fixed circuit traffic load χ) [59].

For circuit holding times that are orders of magnitude larger than the typically packet delays (service times) in the system, the fluctuations of the circuit bandwidth β occur at a significantly longer (slower) time scale than the packet service time scale. That is, the bandwidth β occupied by circuits exhibits significant correlations over time

which in turn give rise to complex correlations with the packet queueing delay [62,72]. For instance, packets arriving during a long period of high circuit bandwidth may experience very long queueing delays and are possibly only served after some circuits release their bandwidth. As illustrated in Section 6.3, the effects of these complex correlations become significant for scenarios with moderate to long circuit holding times $1/\mu$ when the circuit traffic load is low to moderate relative to the circuit bandwidth limit C_c (so that pronounced circuit bandwidth fluctuations are possible), and the packet traffic load on the remaining bandwidth of approximately $C-C_c$ is relatively high, so that substantial packet queue build-up can occur. We leave a detailed mathematical analysis of the complex correlations occurring in these scenarios in the context of DyCaPPON for future research.

In the present study, we focus on an approximate packet delay analysis that neglects the outlined correlations. We base our approximate packet delay analysis on the expectation $E_\beta[f(\beta)]$ (12), i.e., we linearly weigh packet delay metrics $f(\beta)$ with the probability masses $q(\beta)$ for the aggregate circuit bandwidth β. We also neglect the "low-load" operating mode of Section 4.1.1 in the analysis.

In the proposed DyCaPPON cycle structure, a packet experiences five main components, namely (i) the reporting delay from the generation instant of the packet to the transmission of the report message informing the OLT about the packet, which for the fixed cycle duration of DyCaPPON equals half the cycle duration, i.e., $\Gamma/2$, (ii) the report-to-packet partition delay D_{r-p} from the instant of report transmission to the beginning of the packet partition in the next cycle, (iii) the queuing delay D_q from the reception instant of the grant message to the beginning of the transmission of the packet, as well as (iv) the packet transmission delay with mean $\overline{P}/C$, and (v) the upstream propagation delay τ.

In the report-to-packet partition delay we include a delay component of half the mean duration of the packet partition $\overline{G^p}/2$ to account for the delay of the reporting of a particular ONU to the end of the packet partition. The delay from the end of the packet partition in one cycle to the beginning of the packet partition of the next cycle is the maximum of the roundtrip propagation delay 2τ and the mean duration of the circuit partition Ξ. Thus, we obtain overall for the report-to-packet partition delay

$$D_{r-p}=\frac{\overline{G^p}}{2}+\mathbb{E}_\beta\left[\max\left\{2\tau,\ \frac{\beta\Gamma}{C}\right\}\right] \tag{17}$$

$$D_{r-p}=\frac{1}{2}\left(\Gamma+\mathbb{E}_\beta\left[\max\left\{2\tau,\ \frac{\beta\Gamma}{C}\right\}\right]-\omega_o\right). \tag{18}$$

We model the queueing delay with an M/G/1 queue. Generally, for messages with mean service time $\overline{L}/C$, normalized message size variance $\sigma^2/\overline{L}^2$, and traffic intensity ρ, the M/G/1 queue has expected queueing delay [73]

$$D_{M/G/1}=\frac{\rho\frac{\overline{L}}{C}\left(1+\frac{\sigma^2}{\overline{L}^2}\right)}{2(1-\rho)}. \tag{19}$$

For DyCaPPON, we model the aggregate packet traffic from all J ONUs as feeding into one M/G/1 queue with mean packet size $\overline{P}$ and packet size variance σ_p^2. We model the circuit partitions, when the upstream channel is not serving packet traffic, through scaling of the packet traffic intensity. In particular, the upstream channel is available for serving packet traffic only for the mean fraction $(\overline{G^p}-\omega_u)/\Gamma$ of a cycle. Thus, for large backlogs served across several cycles, the packet traffic intensity during the packet partition is effectively

$$\pi_{\text{eff}}=\frac{\pi}{\pi_{\max}}. \tag{20}$$

Hence, the mean queueing delay is approximately

$$D_q=\frac{\frac{\pi_{\text{eff}}\overline{P}}{C}\left(1+\frac{\sigma_p^2}{\overline{P}^2}\right)}{2(1-\pi_{\text{eff}})}. \tag{21}$$

Thus, the overall mean packet delay is approximately

$$D=\frac{\Gamma}{2}+D_{r-p}+D_q+\frac{\overline{P}}{C}+\tau. \tag{22}$$

6. DyCaPPON performance results

6.1. Evaluation setup

We consider an EPON with $J=32$ ONUs, a channel bit rate $C=10$ Gb/s, and a cycle duration $\Gamma=2$ ms. Each ONU has abundant buffer space and a one-way propagation delay of $\tau=96$ μs to the OLT. The guard time is $t_g=5$ μs and the report message has 64 bytes. We consider $K=3$ classes of circuits as specified in Table 2. A packet has 64 bytes with 60% probability, 300 bytes with 4% probability, 580 bytes with 11% probability, and 1518 bytes with 25% probability, thus the mean packet size is $\overline{P}=$ 493.7 bytes. The verifying simulations were conducted with a CSIM based simulator and are reported with 90% confidence intervals which are too small to be visible in the plots.

6.2. Impact of packet traffic load π

In Table 3 we present circuit blocking probability results. In Fig. 4 we plot packet delay results for increasing packet traffic load π. We consider three levels of offered circuit traffic load χ, which are held constant as the packet traffic load π increases. DyCaPPON ensures consistent circuit service with the blocking probabilities and delay characterized in Section 5.1 irrespective of the packet traffic load π, that is, the packet traffic does *not* degrade the circuit service at all. Specifically, Table 3 gives the blocking probabilities B_k as well as the average circuit

Table 2
Circuit bandwidths b_k and request probabilities p_k for $K=3$ classes of circuits in performance evaluations.

Circuit traffic parameters	Class k		
	1	2	3
b_k [Mb/s]	52	156	624
p_k [%]	53.56	28.88	15.56

Table 3
Circuit blocking probabilities B_k from analysis (A) Eq. (10) with representative verifying simulations (S) for given offered circuit traffic load χ, circuit bandwidth limit C_c=2 or 4 Gb/s and mean circuit holding time $1/\mu$. The blocking probabilities are independent of the packet traffic load π. Table also gives average circuit traffic bit rate $\overline{\beta}$ from (13), mean duration of packet phase $\overline{G}_p$ (15), and packet traffic load limit $\pi_{\max}$ (16).

χ	C_c [Gb/s]	$1/\mu$ [s]	B_1 [%]	B_2 [%]	B_3 [%]	$\overline{B}$ [%]	$\overline{\beta}$ [10^9 Gbps]	$\overline{G}_p$ [ms]	$\pi_{\max}$
0.1	4	0.5, A	8.5×10^{-3}	0.031	0.28	0.057	1.05	1.68	0.842
0.1	2	0.02, A	0.93	3.2	21	4.6	0.93	1.70	0.852
0.4	4	0.5, S	3.4	11	41	11	3.0		
0.4	4	0.5, A	3.3	11	40	11	3.02	1.33	0.665
0.4	2	0.02, S	13	35	87	31	1.7		
0.4	2	0.02, A	12	33	86	30	1.68	1.60	0.799
0.7	4	0.5, A	9.6	27	75	25	3.49	1.24	0.618
0.7	2	0.02, A	23	57	98	45	1.83	1.57	0.785

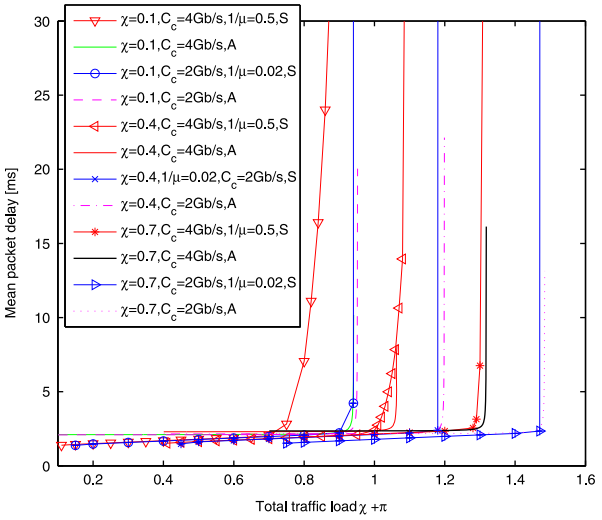

Fig. 4. Impact of packet traffic load π: mean packet delay D from simulations (S) and analysis (A) as a function of total traffic load $\chi+\pi$, which is varied by varying π for fixed circuit traffic load $\chi = 0.1$, 0.4, or 0.7.

blocking probability $\overline{B} = \sum_{k=1}^{K} p_k B_k$ for the different levels of offered circuit traffic load; these blocking probability values hold for the full range of packet traffic loads π.

We observe from Table 3 that for a given offered circuit traffic load level χ, the blocking probability increases with increasing circuit bit rate b_k as it is less likely that sufficient bit rate is available for a higher bit rate circuit. Moreover, we observe that the blocking probabilities increase with increasing offered circuit traffic load χ. This is because the circuit transmission limit C_c becomes increasingly saturated with increasing offered circuit load χ, resulting in more blocked requests. The representative simulation results in Table 3 indicate that the stochastic knapsack analysis is accurate, as has been extensively verified in the context of general circuit switched systems [65].

In Fig. 4 we plot the mean packet delay as a function of the total traffic load, i.e., the sum of offered circuit traffic load χ plus the packet traffic load π. We initially exclude the scenario with $\chi = 0.1$, C_c=4 Gbps, and $1/\mu = 0.5$ s from consideration; this scenario is discussed in Section 6.3. We observe from Fig. 4 that for low packet traffic load π (i.e., for a total traffic load $\chi+\pi$ just above the offered circuit traffic load χ), the packet delay is nearly independent of the offered circuit traffic load χ. For low packet traffic load, the few packet transmissions fit easily into the packet partition of the cycle.

We observe from Fig. 4 sharp packet delay increases for high packet traffic loads π that approach the maximum total traffic load, i.e., offered circuit traffic load χ plus maximum packet traffic load $\pi_{\max}$. For C_c=2 Gb/s, the maximum packet traffic load $\pi_{\max}$ is 0.85 for $\chi = 0.1$ and $\pi_{\max} = 0.79$ for $\chi = 0.7$, see Table 3. Note that the maximum packet traffic load $\pi_{\max}$ depends on the offered circuit traffic load χ and the circuit traffic limit C_c. For a low offered circuit traffic load χ relative to C_c/C, few circuit requests are blocked and the admitted circuit traffic load (equivalently mean aggregate circuit bandwidth $\overline{\beta}$) is close to the offered circuit load χ. On the other hand, for high offered circuit traffic load χ, many circuit requests are blocked, resulting in an admitted circuit traffic load (mean aggregate circuit bandwidth $\overline{\beta}$) significantly below the offered circuit traffic load χ. Thus, the total (normalized) traffic load, i.e., offered circuit load χ plus packet traffic load π, in a stable network can exceed one for high offered circuit traffic load χ.

6.3. Impact of mean circuit holding time

We now turn to the packet delay results for the scenario with low circuit traffic load $\chi = 0.1$ relative to the circuit bandwidth limit C_c=4 Gbps and moderately long mean circuit holding time $1/\mu = 0.5$ s in Fig. 4. We observe for this scenario that the mean packet delays obtained from the simulations begin to increase dramatically as the total load $\chi+\pi$ approaches 0.8. In contrast, for the circuit traffic load $\chi = 0.1$ in conjunction with the lower circuit bandwidth limit C_c=2 Gbps and short mean circuit holding times $1/\mu = 0.02$ s, the mean packet delays remain low for total loads up to close to the total maximum load $\chi+\pi_{\max} = 0.95$ and then increase sharply.

The pronounced delay increases at lower loads (in the 0.75–0.92 range) for the $\chi = 0.1$, C_c=4 Gbps, $1/\mu = 0.5$ s scenario are mainly due to the higher-order complex correlations between the pronounced slow-time scale fluctuations of the circuit bandwidth and the packet queueing as explained in Section 5.2.2. The high circuit bandwidth limit C_c=4 Gbps relative to the low circuit

traffic load $\chi = 0.1$ allows pronounced fluctuations of the aggregate occupied circuit bandwidth β. For the moderately long mean circuit holding time $1/\mu = 0.5$ s, these pronounced fluctuations occur at a long time scale relative to the packet service time scales, giving rise to pronounced correlation effects. That is, packets arriving during periods of high circuit bandwidth β may need to wait (queue) until some circuits end and release sufficient bandwidth to serve the queued packet backlog. These correlation effects are neglected in our approximate packet delay analysis in Section 5.2.2 giving rise to the large discrepancy between simulation and analysis observed for the $\chi = 0.1$, C_c=4 Gb/s, $1/\mu = 0.5$ s scenario in Fig. 4.

We observe from Fig. 4 for the scenarios with relatively high circuit traffic loads $\chi = 0.4$ and 0.7 relative to the considered circuit bandwidth limits C_c=2 and 4 Gbps that the mean packet delays remain low up to levels of the total load close to the total stability limit $\chi + \pi_{\max}$ predicted from the stability analysis in Section 5.2.1. The relatively high circuit traffic loads χ lead to high circuit blocking probabilities (see Table 3) and the admitted circuits utilize the available circuit traffic bandwidth C_c nearly fully for most of the time. Vacant portions of the circuit bandwidth C_c are quickly occupied by the frequently arriving new circuit requests. Thus, there are only relatively minor fluctuations of the bandwidth available for packet service and the approximate packet delay analysis is quite accurate.

Returning to the scenario with relatively low circuit traffic load $\chi = 0.1$ in Fig. 4, we observe that for the short mean circuit holding time $1/\mu = 0.02$, the mean packet delays remain low up to load levels close to the stability limit $\chi + \pi_{\max}$. For these relatively short circuit durations, the pronounced fluctuations of the occupied circuit bandwidth occur on a sufficiently short time scale to avoid significant higher-order correlations between the circuit bandwidth and the packet service.

We examine these effects in more detail in Fig. 5, which shows means and standard deviations of packet delays as a function of the mean circuit holding time $1/\mu$ for fixed traffic load $\chi = 0.5$, $\pi = 0.6$. We observe that for the high C_c=4 Gbps circuit bandwidth limit, the mean packet delay as well as the standard deviation of the packet delay obtained from simulations increase approximately linearly with increasing mean circuit holding time $1/\mu$. The C_c= 4 Gbps circuit bandwidth limit permits sufficiently large fluctuations of the circuit bandwidth β for the $\chi = 0.5$ load, such that for increasing circuit holding time, the packets increasingly experience large backlogs that can only be cleared when some circuits end and release their bandwidth. In contrast, for the lower circuit bandwidth limit C_C=2 Gbps, which severely limits fluctuations of the circuit bandwidth β for the high circuit traffic load $\chi = 0.5$, the mean and standard deviation of the packet delay remain essentially constant for increasing mean circuit holding time $1/\mu$ (and correspondingly decreasing circuit request arrival rate λ_c).

6.4. Impact of offered circuit traffic load χ

In Table 4, we examine the impact of the circuit traffic load χ on the DyCaPPON performance more closely. We keep the packet traffic load fixed at $\pi = 0.7$ and examine the average circuit blocking probability $\overline{B}$ and the mean packet delay D as a function of the circuit traffic load χ. We observe from Table. 4 that, as expected, the mean circuit blocking probability $\overline{B}$ increases with increasing circuit traffic load χ, whereby analysis closely matches the simulations.

For the packet traffic, we observe from Table 4 a very slight increase in the mean packet delays D as the circuit traffic load χ increases. This is mainly because the transmission rate limit C_c for circuit service bounds the upstream transmission bandwidth the circuits can occupy to no more than C_c in each cycle. As the circuit traffic load χ increases, the circuit traffic utilizes this transmission rate limit C_c more and more fully. However, the packet traffic is guaranteed a portion $1 - C_c/C$ of the upstream transmission bandwidth. Formally, as the circuit traffic load χ grows large ($\chi \to \infty$), the mean aggregate circuit bandwidth $\overline{\beta}$ approaches the limit C_c, resulting in a lower bound for the packet traffic load

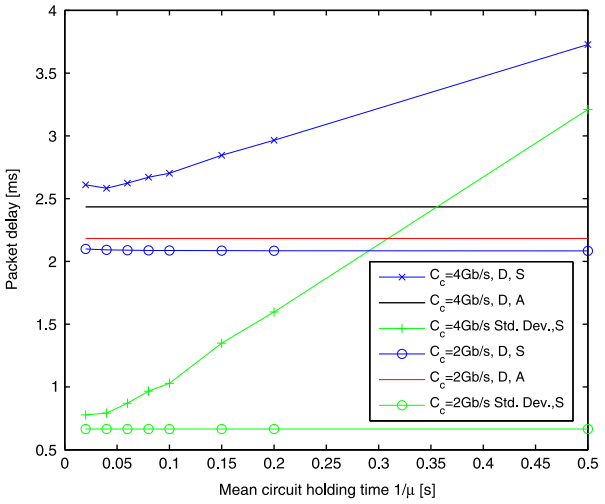

Fig. 5. Mean packet delay D and standard deviation of packet delay as a function of mean circuit holding time $1/\mu$; fixed parameters $\chi = 0.5$, $\pi = 0.6$.

limit (16) of $\pi_{\max}=1-\max\{2\tau/\Gamma,\ C_c/C\}-(\omega_o+\omega_u)/\Gamma$ and corresponding upper bounds for the effective packet traffic intensity π_{eff} and the mean packet delay D.

6.5. Impact of limit C_c for circuit service

In Fig. 6 we examine the impact of the transmission rate limit C_c for circuit traffic. We consider different compositions χ, π of the total traffic load $\chi+\pi=1.05$. We observe from Fig. 6(a) that the average circuit blocking probability $\overline{B}$ steadily decreases for increasing C_c. In the example in Fig. 6, the average circuit blocking probability $\overline{B}$ drops to negligible values below 1% for C_c values corresponding to roughly twice the offered circuit traffic load χ. For instance, for circuit load $\chi=0.25$, $\overline{B}$ drops to 0.9% for $C_c=5$ Gb/s. The limit C_c thus provides an effective parameter for controlling the circuit blocking probability experienced by customers.

From Fig. 6(b), we observe that the mean packet delay abruptly increases when the C_c limit reduces the packet traffic portion $1-C_c/C$ of the upstream transmission bandwidth to values near the packet traffic intensity π. We also observe from Fig. 6(b) that the approximate packet delay analysis is quite accurate for small to moderate C_c values (the slight delay overestimation is due to neglecting the low packet traffic polling), but underestimates the packet delays for large C_c. Large circuit traffic limits C_c give the circuit traffic more flexibility for causing

Table 4
Mean circuit blocking probability $\overline{B}$ and mean packet delay D as a function of circuit traffic load χ; fixed parameters: circuit bandwidth limit $C_c=2$ Gb/s, packet traffic load $\pi=0.7$.

χ	0.0001	0.05	0.1	0.20	0.40	0.60	$\chi\to\infty$
$\overline{B}$, S [%]	0	1.2	5.1	16	31	43	
$\overline{B}$, A [%]	0.016	1.08	4.81	14.9	29.6	40.1	100
D, S [ms]	1.9	2.0	2.0	2.1	2.2	2.2	
D, A [ms]	2.10	2.11	2.13	2.16	2.21	2.23	2.42

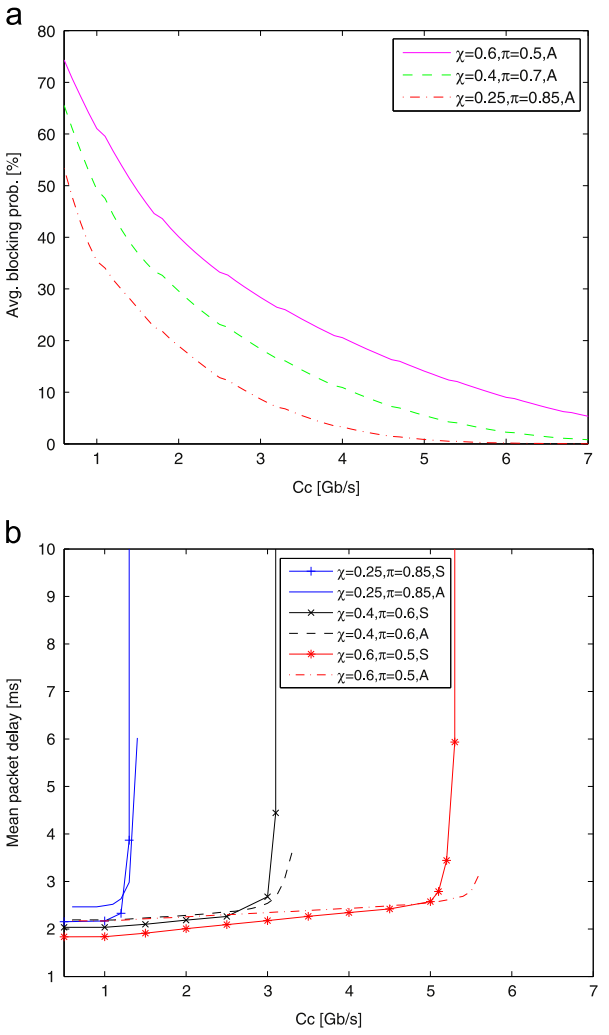

Fig. 6. Impact of circuit service limit C_c: mean circuit blocking probability $\overline{B}$ (from analysis, Eq. (10)) and mean packet delay D (from analysis and simulation) as a function of transmission rate limit for circuit service C_c; fixed mean circuit holding time $1/\mu=0.02$ s. (a) Mean request blocking probability $\overline{B}$. (b) Mean packet delay D.

fluctuations of the occupied circuit bandwidth, which deteriorate the packet service. Summarizing, we see from Fig. 6(b) that as the effective packet traffic intensity $\pi/(1-C_c/C)$ approaches one, the mean packet delay increases sharply. Thus, for ensuring low-delay packet service, the limit C_c should be kept sufficiently below $(1-\pi)C$.

When offering circuit and packet service over shared PON upstream transmission bandwidth, network service providers need to trade off the circuit blocking probabilities and packet delays. As we observe from Fig. 6, the circuit bandwidth limit C_c provides an effective tuning knob for controlling this trade-off.

7. Conclusion

We have proposed and evaluated DyCaPPON, a passive optical network that provides dynamic circuit and packet service. DyCaPPON is based on fixed duration cycles, ensuring consistent circuit service, that is completely unaffected by the packet traffic load. DyCaPPON masks the round-trip propagation delay for polling of the packet traffic queues in the ONUs with the upstream circuit traffic transmissions, providing for efficient usage of the upstream bandwidth. We have analyzed the circuit level performance, including the circuit blocking probability and delay experienced by circuit traffic in DyCaPPON, as well as the bandwidth available for packet traffic after serving the circuit traffic. We have also conducted an approximate analysis of the packet level performance.

Through extensive numerical investigations based on the analytical performance characterization of DyCaPPON as well as verifying simulations, we have demonstrated the circuit and packet traffic performance and trade-offs in DyCaPPON. The provided analytical performance characterizations as well as the identified performance trade-offs provide tools and guidance for dimensioning and operating PON access networks that provide a mix of circuit and packet oriented service.

There are several promising directions for future research on access networks that flexibly provide both circuit and packet service. One important future research direction is to broadly examine cycle-time structures and wavelength assignments in PONs providing circuit and packet service. In particular, the present study focused on a single upstream wavelength channel operated with a fixed polling cycle duration. Future research should examine the trade-offs arising from operating multiple upstream wavelength channels and combinations of fixed- or variable-duration polling cycles. An exciting future research direction is to extend the PON service further toward the individual user, e.g., by providing circuit and packet service on integrated PON and wireless access networks, such as [74–78], that reach individual mobile users. Further, exploring combined circuit and packet service in long-reach PONs with very long round trip propagation delays, which may require special protocol mechanisms, see e.g., [79–81], is an open research direction. Another direction is to examine the integration and interoperation of circuit and packet service in the PON access network with metropolitan area networks [82–85] and wide area networks to provide circuit and packet service [17].

Appendix A

A.1. Evaluation of equilibrium probabilities $q(\beta)$

In this Appendix, we present the recursive Kaufman–Roberts algorithm [65, p. 23] for computing the equilibrium probabilities $q(\beta)$, $0 \le \beta \le C_c$, that the currently active circuits occupy an aggregated bandwidth β. For the execution of the algorithm, the given circuit bandwidths $b_1, b_2, \ldots, b_K$ and limit C_c are suitably normalized so that incrementing β in integer steps covers all possible combinations of the circuit bandwidths. For instance, in the evaluation scenario considered in Section 6.1, all circuit bandwidths are integer multiples of 52 Mb/s. Thus, we normalize all bandwidths by 52 Mb/s and for e.g., C_c=5 Gb/s execute the following algorithm for $\beta = 0, 1, 2, \ldots, 96$. (The variables b_k, C_c, and β refer to their normalized values, e.g., C_c=96 for the C_c=5 Gb/s example, in the algorithm below).

The algorithm first evaluates unnormalized occupancy probabilities $g(\beta)$ that relate to a product-form solution of the stochastic knapsack [65]. Subsequently the normalization term G for the occupancy probabilities is evaluated, allowing then the evaluation of the actual occupancy probabilities $q(\beta)$.

1. Set $g(0) \leftarrow 1$ and $g(\beta) \leftarrow 0$ for $\beta < 0$.
2. For $\beta = 1, 2, \ldots, C_c$, set
$$g(\beta) \leftarrow \frac{1}{\beta} \sum_{k=1}^{K} \frac{b_k p_k \lambda_c}{\mu} g(\beta - b_k). \tag{23}$$
3. Set
$$G = \sum_{\beta=0}^{C_c} g(\beta). \tag{24}$$
4. For $\beta = 0, 1, \ldots, C_c$, set
$$q(\beta) \leftarrow \frac{g(\beta)}{G}. \tag{25}$$

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